

### 802.3 PoE Specification Parameters

802.3 PoE Parameter	Parameter Description	802.3af Section	802.3at Section	PSE Conformance Test
<b>Voc</b>	Open Circuit Detection Voltage (peak)	<b>Table 33-2</b>	<b>Table 33-4</b>	<b>det_v</b>
<b>Vvalid (max)</b>	Maximum Detection Voltage with Valid Detection Load			
<b>Vvalid (min)</b>	Minimum Detection Step Voltage with Valid Detection Load			
<b>ΔVtest</b>	Maximum Detection Pulse Voltage Step Size			
<b>Vslew</b>	Maximum Slew Rate of Valid Detection Pulse Step			
<b>Pulse_Steps</b>	Minimum Valid Detection Voltage Transitions			
<b>Isc (init)</b>	Short Circuit Current Limit During Detection @ < 2.8 V	<b>Table 33-2</b>	<b>Table 33-4</b>	<b>det_i</b>
<b>Isc (det)</b>	Short Circuit Current Limit During Detection @ > 2.8 V			
<b>Rgood_max</b>	Maximum Valid Detection Resistance	<b>Table 33-2</b>	<b>Table 33-4</b>	<b>det_range</b>
<b>Rgood_min</b>	Minimum Valid Detection Resistance			
<b>Cgood_max</b>	Maximum Valid Detection Capacitance			
<b>Tdbo</b>	Detection Back-Off Time Apparent from Signaling Time from Final Detection Pulse (invalid load) until Final Detection Pulse preceding power-up with valid signature 802.3af Detection Pulse Duration	<b>33.2.3.1</b>	<b>33.2.4.1</b>	<b>det_time</b>
<b>Tdbo_Effective</b>				
<b>Tdet</b>		<b>33-5</b>	<b>33-9</b>	
<b>Zout</b>	PSE Effective Output Impedance during Detection	<b>33.2.5</b>	<b>33.2.6</b>	<b>det_resource</b>
<b>Vclass</b>	Peak Classification Voltage	<b>33.2.7.2</b>	<b>Table 33-8</b>	<b>class_v</b>
<b>Vmark</b>	Mark Event Voltage (2-Event Classification)	<b>N/A</b>		
<b>Tpdc</b>	Total Classification Pulse (Measurement) Duration	<b>Table 33-5</b>	<b>Table 33-5 &amp; 33-8</b>	<b>class_time</b>
<b>Event Count</b>	Count of Classification Pulses (Measurements)	<b>33.2.7</b>		
<b>Tcle1</b>	Duration of 1 <sup>st</sup> Classification Measurement (2-Event Class)	<b>N/A</b>		
<b>Tcle2</b>	Duration of 2 <sup>nd</sup> Classification Measurement (2-Event Class)			
<b>Tme1</b>	Duration of 1 <sup>st</sup> Mark Region (2-Event Class)			
<b>Tme2</b>	Duration of 2 <sup>nd</sup> Mark Region (2-Event Class)			
<b>Trise</b>	Power-On Rise Time / Turn On Ramp Rate	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrup_time</b>
<b>Tpon</b>	Power-On Timing from End of Detection to Power-Up			
<b>Inrush (Max)</b>	Maximum In-Rush Current during Power-Up (after 1 msec)	<b>Table 33-5, 33.2.8.5</b>	<b>Table 33-9, 33.2.9.6</b>	<b>pwrup_inrush</b> <i>pwrup_inrush_2</i>
<b>Inrush (Min)</b>	Minimum In-Rush Current Capacity			
<b>Tinrush</b>	PSE Time to Power Removal on Inrush Overload			
<b>Vport</b>	DC Port Voltage	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrup_v</b>
<b>Vpp (low band)</b>	AC Ripple Voltage 16 Hz to 5 KHz			
<b>Vpp (high band)</b>	AC Noise Voltage (p-p) 5KHz – 300 KHz	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrup_noise</b>
<b>Pport Capacity</b>	PSE Port Power Delivery Capacity	<b>Table 33-5</b>	<b>Table 33-6</b> <b>33.2.9.5</b>	<b>pwrup_pwracap</b> <i>pwrup_pwracap_2</i>
<b>Iport Capacity</b>	PSE Output Current Capacity at Max Power	<b>33.2.8.4</b>		
<b>Ilim (Max)</b>	Maximum (Short Circuit) Current from 1 msec to 75 msec	<b>Table 33-5</b>	<b>Table 33-9, 33.2.9.9</b>	<b>pwrup_maxi</b> <i>pwrup_maxi_2</i>
<b>Ilim (Min)</b>	Minimum (Short Circuit) Current from 0 msec to 50 msec			
<b>Tiim</b>	Time to Power Removal on Short Circuit Overload			
<b>Vport_Min</b>	Minimum Port Voltage Given Load Step < Ilim	<b>33.2.8.4</b>	<b>33.2.9.5</b>	<b>pwrup_overld</b> <i>pwrup_overld_2</i>
<b>Negative_Slew</b>	Negative Going Voltage Slew Rate Given Load Step < Ilim	<b>33.2.8.2</b>	<b>33.2.9.2</b>	
<b>Positive_Slew</b>	Positive Going Voltage Slew Rate Given Load Step < -Ilim			
<b>Tmpdo</b>	Disconnect Power-Down Timing (AC MPS)	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>mpps_ac_pwrnd</b>
<b>V_open</b>	Peak-Peak AC MPS Voltage (open circuit) as V and %Vport AC MPS Frequency AC MPS Signal Slew Rate AC MPS Source Current Compliance (Limit)	<b>Table 33-6</b>	<b>Table 33-10</b>	<b>mpps_ac_vf</b>
<b>Fp</b>				
<b>MPS Slew SR</b>				
<b>I_sac</b>				
<b>V_open1</b>	Peak Detection Voltage following Power Removal Maximum port voltage recorded after PD disconnect event	<b>Table 33-6</b>	<b>Table 33-10</b>	<b>mpps_ac_voff</b>
<b>Vport(max)</b>				

PowerSync Analyzer  
**802.3 PSE Conformance Test Coverage**  
*PSE Conformance Test Version 3.5.xx*



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<b>Imin2 Tmps</b>	Minimum current to keep power alive in DC MPS PSE's Minimum Imin2 ON Time Required for DC MPS Validity	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>mps_dc_valid</b>
<b>Imin1 Tmpdo</b>	Maximum (low) current where PSE must remove power Disconnect Power-Down Timing (DC MPS)	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>mps_dc_pwrnd</b>
<b>Icut Tovld</b>	Overload Cut-Off Current Time to Power Removal on Overload and Short Circuit	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrnd_ovld</b>
<b>Toff Cout</b>	Power-Down Timing (into effective 320Kohm load) PSE Port Capacitance with Power Removed	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrnd_time</b>
<b>Voff Ted</b>	IDLE State Average Voltage (between detections) Power-Up Inhibition Time following Overload Shutdown	<b>Table 33-5</b>	<b>Table 33-9</b>	<b>pwrnd_v pwrnd_v_2</b>

## 2) Additional PSE Conformance Test Parameters

802.3af Parameter	Parameter Description	PSE Conformance Test
<b>Non_802_Step_V High_Sig_MaxV Non_802_Discr</b>	Peak IDLE State Voltage Level (including non-valid detection steps) Peak Detection Pulse Voltage w/ Marginally High Detection Signature "1" indicates PSE Port is using proprietary (non-802.3) detection methods to disqualify near-valid detection signatures	<b>det_v</b>
<b>Detect_Strategy</b>	Categorizes PSE Open Circuit Detection method as one of: 0: Normal 802.3 discrete detection measurements 1: Proprietary Pre-Detection ("qualification") Measurements 2: Continuously Measuring with No Backoff 3: Mixed 802.3 and Discrete Proprietary Legacy Detection Pulses 4: Continuously Measuring with No Backoff Above 10V	
<b>Backoff_Type</b>	Categorizes PSE Detection Backoff method as one of: 0: Normal 802.3 detection – exclusively 802.3 detection pulses 1: Mixed 802.3 detection and proprietary detection pulses 2: Mixed 802.3 detection and proprietary higher voltage legacy detection pulses	<b>det_time</b>
<b>Total_Det_Time</b>	Total Detection Measurement Duration Including Non-Conformant Voltage Steps	
<b>Inrush (Init) Inrush_Voltage Powered_Vport</b>	Maximum In-Rush Current over first 1 msec of Inrush Overload Port voltage during condition of Inrush Overload Port voltage following a 25 msec current-limiting Inrush Overload	<b>pwrup_inrush pwrup_inrush_2</b>
<b>DC_Power_Pport DC_Current_Iport</b>	Port Power Given 2.4 Watt Load Port Current Given 2.4 Watt Load	<b>pwrup_pwr</b>
<b>Pport Class</b>	Maximum Guaranteed PD Classification Supported	<b>pwrup_pwracap pwrup_pwracap_2</b>
<b>Ilim (Init) Output_Voltage_V 25msec_Short_Vport</b>	Maximum Short-Circuit Current over first 1 msec of Overload Average DC Voltage over Duration of Short Circuit Overload Port Response following a 25 msec Duration Short Circuit Overload	<b>pwrup_maxi pwrup_maxi_2</b>
<b>Power Duration Integ_Power_Out</b>	Valid (> Vport_Min) Voltage Duration given 3msec Load Step < Ilim Integrated Power (Energy) Delivered during 3msec Load Step < Ilim	<b>pwrup_overld pwrup_overld_2</b>
<b>Imin1</b>	Maximum DC Load Current Present AC MPS PSE Disconnect	<b>mps_ac_pwrnd</b>
<b>V_open1</b>	Peak Detection Voltage following Power Removal with DC MPS PSE	<b>mps_dc_pwrnd</b>
<b>Rp</b>	PSE Port Shunt Load Resistance During Power-Down.	<b>pwrnd_time</b>
<b>Ved</b>	Peak Voltage Over the Minimum Ted Time Interval Following Error Condition.	<b>pwrnd_v pwrnd_v_2</b>

For PSE Conformance Test Suite (version 4.x.xx) 802.3at Coverage, see:  
[Sifos Technologies, 802.3at PSE PICS Coverage.pdf](#).